

## HLRS-Intel oneAPI HPC Workshop

September 13<sup>th</sup> 2023 Sneha Chattopadhyay



## Objectives

- Get to know / Learn / Understand :
  - The oneAPI programming model
  - Building applications with DPC++/SYCL
  - Fundamentals of OpenMP offloading
  - How to use Intel's oneAPI libraries (oneMLK, ...) and APIs
  - Intel's heterogenous profiling and performance analysis tools
  - A basic understanding on (dynamical) debugging of applications using the oneAPI programming model
  - Intel's Compatibility tool that helps to migrate CUDA to SYCL code.

## AGENDA Day 1 : Sept 13<sup>th</sup> 2023

Start T	End Time	Duratior	Торіс	Presenter	Chair for Q&A
9:00	9:10	0:10	Welcome and Introduction to Day 1	Tobias Haas (HLRS) and Sneh	a Chattopadhyay (Intel)
9:10	9:30	0:20	oneAPI – Introduction to a mixed Architecture Development Environment		
			- Motivation and oneAPI Standardization	Sneba Chattonadhyay (Intel)	Edmund (Intel)
			- Intel's oneAPI Toolkits Portfolio and Components	Sheha chattopadhyay (inter)	Luniana (inter)
			- Intel oneAPI plug-ins for Nvidia and AMD hardware ( CPU and GPUs)		
9:30	10:20	0:50	Direct programming with oneAPI Compilers (Part 1) – with Demos		
			- Intro to heterogenous programming model with SYCL 2020		
			- SYCL features and examples		
			o "Hello World" Example	Igor Vorobtsov (Intel)	Alina Shadrina (Intel)
			o Device Selection		
			o Execution Model		
10:20	10:25	0:05	Break		
10:25	11:15	0:50	Direct programming with oneAPI Compilers (Part 2) – with Demos		
			o Compilation and Execution Flow		
			o Memory Model; Buffers, Unified Shared Memory (USM)	Igor Vorobtsov (Intel)	Alina Shadrina (Intel)
			o Performance optimizations with SYCL features	Ū , ,	
11:15	11:20	0:05	Break	-	
11:20	12:20	1:00	oneAPI Case Study – GROMACS (50 minutes talk + 10 minutes Q&A)	Andrey Alekseenko (KTH)	Heinrich Bockhorst (Intel)
12:20	12:25	0:05	Break		
12:25	12:45	0:20	Introduction to the DevCloud/ IDC - A sandbox for software development and benchmarking	Heinrich Bockhorst (Intel)	Fabio Baruffa (Intel)
12:45	13:05	0:20	Instructions on lab exercises (direct programming with SYCL using Intel oneAPI compilers)	Igor Varabtsov (Intel)	Matthias Kirchhart (Intel)
					Mattinas Kircinart (inter)
13:05	14:05	1:00	Lunch		
14:05	15:20	1:15	Self-paced hands-on with Intel technical consultancy and support via Slack	Alina Shadrina (Intal) Igar Varahta	www.(Intel) Matthias Kirabbart
				Alina Shadina (inter), igor vorobis	ov (inter), Matthias Kirchhart
				(inter)	
15:20	15:50	0:30	Break		
15:50	17:05	1:15	Self-paced hands-on with Intel technical consultancy and support via Slack	Alina Shadrina (Intel), Igor Vorobts	ov (Intel) Matthias Kirchhart
				(Intel)	(inter), Matthias Ritelliar
				(inter)	1

## AGENDA Day 2 : Sept 14<sup>th</sup> 2023

			TOPIC	PRESENTER	Chair for Q&A	
9:00	9:05	0:05	Welcome and Introduction to Day 2	Tobias Haas (HLRS) and Sneh	a Chattopadhyay (Intel)	
9:05	9:55	0:50	Intel OpenMP for Offloading for Fortran – with Demos - Parallelizing heterogenous applications with OpenMP 5.2			
9:55	10:00	0:05	Break			
10:00	10:35	0:35	Intel oneAPI libraries (oneMKL) for HPC - with demos - Performance optimized libraries for numerical simulations and other purposes	Matthias Kirchhart (Intel)	Gennady Fedorov(Intel)	
10:35	10:45	0:10	Instructions on lab exercises/ Q&A			
10:45	10:50	0:05	Break			
10:50	11:30	0:40	Target NVIDIA and AMD with oneAPI and SYCL Using SYCL based NVIDIA and AMD plugins with Demos	Rafal Bielski (Codeplay/ Intel)	Matthias Kirchhart (Intel)	
11:30	12:00	0:30	Open Source Compatibility tool for porting purposes(SYCLomatic) - with demo - Migration Cuda based GPU Applications to SYCL Igor			
12:00	12:05	0:05	Break	•	•	
12:05	12:30	0:25	Intel Debugging Tools for heterogenous programming ( CPU, GPU ) - with demos	Pascal Rene Baehr (Intel)	Alina Shadrina (Intel)	
12:30	13:00	0:30	Programming for Distributed HPC Systems using Intel MPI Dmitry Sivkov (Intel) Tobias			
13:00	14:00	1:00	Lunch			
14:00	15:15	1:15	Self-paced hands-on with Intel technical consultancy and support via Slack	Alina, Tobias Kloeffel, Matthias, G Rafae	ennady, Igor, Pascal, Dmitry, I	
15:15	15:45	0:30	Break			
15:45	16:30	0:45	Self-paced hands-on with Intel technical consultancy and support via Slack	Alina, Tobias Kloeffel, Matthias, G Rafae	ennady, Igor, Pascal, Dmitry, I	

4

## AGENDA Day 3 : Sept 15<sup>th</sup> 2023

			ТОРІС	PRESENTER	Chair for Q&A		
9:00	9:05	0:05	Welcome and Introduction to Day 3	Tobias Haas (HLRS) and Sneha Chattopadhyay (In			
9:05	10:05	1:00	Application profiling for CPU and or mixed hardware withe the Intel VTune - Demos				
			<ul> <li>Vtune general / main functionality (Hot spot analysis ,) starting with CPU</li> </ul>				
			- Profiling Tools Interfaces for GPU				
40.05	40.40	0.05	- Profile heterogenous SYCL/OpenMP Workloads with Intel VTune Profiler	Heinrich Bockhorst (Intel)	Rafael Lago (Intel)		
10:05	10:10	0:05	Break	1			
10:10	11:10	1:00	Application profiling for CPU and or mixed hardware withe the INtel VTune - Demos				
			<ul> <li>Vtune general / main functionality (Hot spot analysis ,) starting with CPU</li> </ul>				
			- Profiling Tools Interfaces for GPU				
			- Profile heterogenous SYCL/OpenMP Workloads with Intel VTune Profiler	Heinrich Bockhorst (Intel)	Rafael Lago (Intel)		
11:10	11:20	0:10	Instructions on lab exercises				
11:20	11:25	0:05	Break		•		
11:25	12:25	1:00	Application profiling for CPU and mixed hardware with the Intel Advisor - Demos				
			- Advisor's main functionality (Vectorization and Roofline) starting with CPU				
			- Estimate performance potential gains with Offload Advisor ( CPU -> HW Accelerator)				
			- Analyse heterogenous SYCL/OpenMP Workloads with Intel Advisor and Roofline analysis	is SYCL/OpenMP Workloads with Intel Advisor and Roofline analysis			
				Dmitry Sivkov (Intel)	Heinrich Bockhorst (Intel)		
12:25	12:35	0:10	Intructions on lab exercises				
12:35	12:45	0:10	Q&A and Wrap-Up				
12:45	13:45	1:00	Lunch				
13:45	14:45	1:00	Self-paced hands-on with TCE support via Slack				
				Heinrich Bockhorst, Dmitry Sivkov	, Rafael Lago, Tobias Kloeffel		
				(Intel	_		
14:45	15:05	0:20	Break				
15:05	16:05	1:00	Self-paced hands-on with TCE support via Slack	Heinrich Bockhorst, Dmitry Sivkov	Rafael Lago, Tobias Kloeffel		
				(Intal	, rtalaer Lago, robias rtibeller		
				(inter			

## Call to Action

- Data Centre Admins
  - Prepare and Update your data center with performance optimized Intel oneAPI Toolkits to serve your users and developers
- Developers
  - Use your knowledge about Intel oneAPI Toolkits for application(s) development
  - Move CUDA code to SYCL
  - Develop applications with new LLVM based Intel C++ (ICX) and Fortran (IFX) Compilers
  - Practice with exercises available on Intel Developer Cloud



## oneAPI -

## A new Development Environment

September 13<sup>th</sup> 2023 Sneha Chattopadhyay

sneha.chattopadhyay@intel.com



## Notices & Disclaimers

Performance varies by use, configuration and other factors. Learn more at www.Intel.com/PerformanceIndex. Results may vary.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Slide 50 - Texas Advanced Computing Center (TACC) Frontera references

Article: <u>HPCWire: Visualization & Filesystem Use Cases Show Value of Large Memory Fat Notes on Frontera</u>. www.intel.com/content/dam/support/us/en/documents/memory-and-storage/data-center-persistent-mem/Intel-Optane-DC-Persistent-Memory-Quick-Start-Guide.pdf software.intel.com/content/www/us/en/develop/articles/introduction-to-programming-with-persistent-memory-from-intel.html wreda.github.io/papers/assise-osdi20.pdf

#### **KFBIO**

KFBIO m. tuberculosis screening detectron2 model throughput performance on 2nd Intel® Xeon® Gold 6252 processor: NEW: Test 1 (single instance with PyTorch 1.6: Tested by Intel as of 5/22/2020. 2-socket 2nd Gen Intel® Xeon® Gold 6252 Processor, 24 cores, HT On, Turbo ON, Total Memory 192 GB (12 slots/16 GB/2666 MHz), BIOS: SSE5C620.86B.02.01.0008.031920191559 (ucode: 0x500002c), Ubuntu 18.04.4 LTS, kernel 5.3.0-51-generic, mitigated Test 2 (24 instances with PyTorch 1.6: Tested by Intel as of 5/22/2020. 2-socket 2nd Gen Intel Xeon Gold 6252 Processor, 24 cores, HT On, Turbo ON, Total Memory 192 GB (12 slots/16 GB/2666 MHz), BIOS: SSE5C620.86B.02.01.0008.031920191559 (ucode: 0x500002c), Ubuntu 18.04.4 LTS, kernel 5.3.0-51-generic, mitigated BASELINE: (single instance with PyTorch 1.4): Tested by Intel as of 5/22/2020. 2-socket 2nd Gen Intel Xeon Gold 6252 Processor, 24 cores, HT On, Turbo ON, Total Memory 192 GB (12 slots/16 GB/2666 MHz), BIOS: SSE5C620.86B.02.01.0008.031920191559 (ucode: 0x500002c), Ubuntu 18.04.4 LTS, kernel 5.3.0-51-generic, mitigated BASELINE: (single instance with PyTorch 1.4): Tested by Intel as of 5/22/2020. 2-socket 2nd Gen Intel Xeon Gold 6252 Processor, 24 cores, HT On, Turbo ON, Total Memory 192 GB (12 slots/16 GB/2666 MHz), BIOS: SSE5C620.86B.02.01.0008.031920191559 (ucode: 0x500002c), Ubuntu 18.04.4 LTS, kernel 5.3.0-51-generic, mitigated BASELINE: (single instance with PyTorch 1.4): Tested by Intel as of 5/22/2020. 2-socket 2nd Gen Intel Xeon Gold 6252 Processor, 24 cores, HT On, Turbo ON, Total Memory 192 GB (12 slots/16 GB/2666 MHz), BIOS: SSE5C620.86B.02.01.0008.031920191559 (ucode: 0x500002c), Ubuntu 18.04.4 LTS, kernel 5.3.0-51-generic, mitigated.

#### **Tangent Studios**

Con<sup>7</sup>figurations for Render Times with Intel® Embree, testing conducted by Tangent Animation Labs. Render farm: 8x Intel® Core<sup>™</sup> processors +hyperthread\*2 + 128gig. In-office workstations: Intel® Xeon® processors HP blade c7000 chassis, with HP460 gen8 blades - 2x Intel Xeon E5-2650 V2, Eight Core 2.6GHz-128GB. Software: Blender 2.78 with custom build using Intel® Embree. For more information on Tangent's work with Embree, watch this video: www.youtube.com/watch?time\_continue=251&v=\_2la4h8q3xs&feature=emb\_logo

Recreation of the performance numbers can be recreated using Agent327, Blender and Embree.

#### Chaos Group - Up to 90% Memory Reduction for Displacement

Testing conducted by Chaos Group with Intel<sup>®</sup> Embree 2020. Software Corona Renderer 5 with Intel Embree. Up to 90% memory reduction calculated using Corona Renderer 5 with regular displacement grids per triangle of 154 bytes versus Corona Renderer 5 with Intel Embree, which has a displacement capability grid of 12 bytes per grid triangle. (12/154 = 7.8% usage or >90% memory reduction.) Recreation of the performance numbers can be accomplished using Corona Renderer 5 and Embree. For more information, visit the Corona Renderer Blog: <u>blog.corona-renderer.com/corona-renderer.5-for-3ds-max-released/</u>

#### The Addams Family 2 - Gained a 10% to 20%—and sometimes 25%—efficiency in rendering, saving thousands of hours in rendering production time.

Testing Date: Results are based on data conducted by Cinesite 2020-21. 10% to up to 25% rendering efficiency/thousands of hours saved in rendering production time/15 hrs per frame per shot to 12-13 hrs. Cinesite Configuration: 18-core Intel® Xeon® Scalable processors (W-2295) used in render farm, 2nd gen Intel Xeon processor-based workstations (W-2135 and -2195) used. Rendering tools: Gaffer, Arnold, along with optimizations by Intel® Open Image Denoise.

Your costs and results may vary.

Intel technologies may require enabled hardware, software or service activation.

Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.

© Intel Corporation. Intel, the Intel logo, Xeon, Core, VTune, OpenVINO, Agilex, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

## Agenda

- A Glimpse on Future Evolution of the HPC Computer Architecture
- oneAPI Concept and the need for Standardization for heterogenous Programming
  - SYCL and Data Parallel C++
- The Intel® oneAPI Toolkits and Software Development Components
  - Key oneAPI Tool Components
- Examples of oneAPI Enabling & Workload Migration Activities
- Miscellenous / oneAPI Resources and useful links

How does a machine look like in a heterogenous world?

## Sharing Parallism between CPU and additional Accelerators



How does a machine look like in a heterogenous world?

## A mix of different Accelerators- All running in parallel



## How does a machine look like in a heterogenous world?



mem

GPU

mem

mem

GPU

mem

Can we really program XPUs (acceleration)?

- 1. Freedom = Choice of XPUs
- 2. Value = Maintain Performance across XPUs
- 3. Trustworthy = Maintain One Source Code for Future XPUs

## Solving Developer Challenges

Different languages & toolchains per architecture | single vendor proprietary lock-in limits code reuse | time-consuming & costly development



**Accelerated Programming Made Easier** 

#### Accelerating Choice with SYCL **Khronos Group Standard**

- Open, standards-based
- Multiarchitecture performance
- Freedom from vendor lock-in
- Comparable performance to native CUDA on Nvidia GPUs
- Extension of widely used C++ language
- Speed code migration via open source SYCLomatic or Intel<sup>®</sup> DPC++ Compatibility Tool



Testing Date: Performance results are tanenforcimitivity inclusion of August 35, 2022 and may not refined all publicly availables pointer

Configuration Databased Workbased Settings Path Network 1920 (PLU P2 40Hz, 2 society, Hyper TrimutOn, Tutos Ov, 25508 Here: 2004-3033, society D-2003053, GPU Hardis ADDPON B008 GPU removery Software: 37/CL appr. asses/CLANG/SDD CLCA (DCT/WE/M/DA/W/CCT/H (A/MAK/T) (DDM/T) (down/DDM) TVC) (per second/LANS) complex sectors, hcpc/rangete-reptor/weber ast, MCA/W/C complex sectors; -03 - per code archiveorgane. BC code-ent. BC RepresentativeOkloads with their optimizations.

Performance results are haven' entiting as of dates shown in configurations and may not referring addick available updates. See configuration declass are for details. No product or component can be abanitably anounce

Performance varies by one configuration, and other lactors. Learn more all your biologin Performance at allos. Your context and multi-insig vary

#### **Architectures**

Intel | Nvidia | AMD CPU/GPU | RISC-V | ARM Mali | PowerVR | Xilinx

## oneAPI Open Ecosystem Progress

Open, Broad, Multiarchitecture / Multivendor Implementation



	2020	2021	2022	2023				
	Specification updates							
Initiative & Technology Advancements	oneAPI SYCL implementation Intel CPU, GPU, FPGA support SYCL for Nvidia GPU	Fugaku deploys one Univ. of Heidelberg SYCL for AMD CPUS NERSC, Argonne de for NVIDIA GPU Argonne, Oakridge deploy SYCL for AM	DNN for ArmHardware implementations Arm CPUsdeploys s & GPUsGROMACS SYCL code on Huawei CCE & Ascend use oneAPI community forum oneAPI plug-ins for NVIDI Julia interface to oneAPI TensorFlow accelerates m	s: NVIDIA GPUs, AMD CPUs/GPUs, Intel CPUs/GPUs, NVIDIA & AMD GPUs es oneAPI & open governance established A & AMD odels via oneDNN				
			SYCL performance match	es NVIDIA/AMD native system languages				

Adoption is Growing – Showcased in DevSummits, IWOCL, ISC, SC, AI Conferences...

#### Intel<sup>®</sup> Developer Tools Supporting oneAPI A complete set of proven tools expanded from CPU to accelerators

- Advanced compilers, libraries, and analysis, debug, and porting tools
- Full support for C, C++ with SYCL, Python, Fortran, MPI, OpenMP
- Intel<sup>®</sup> Advisor determines device target mix before you write your code
- Intel's compilers optimize code to take full advantage of multiarchitecture workload distribution.
- Intel<sup>®</sup> VTune<sup>™</sup> Profiler analyzes hotspots to optimize code performance
- Intel AI tools support acceleration of major deep learning and machine learning frameworks

17





## Data Parallel C++

Standards-based, Most Comprehensive, Cross-architecture Implementation of SYCL

DPC++ = ISO C++ and Khronos SYCL and community extensions

#### Freedom of Choice: Future-Ready Programming Model

- Allows code reuse across hardware targets
- Permits custom tuning for a specific accelerator
- Open, cross-industry alternative to proprietary language

## DPC++ = ISO C++ and Khronos SYCL and community extensions

- Designed for data parallel programming productivity
- Provides full native high-level language performance on par with standard C++ and broad compatibility
- Adds SYCL from the Khronos Group for data parallelism and heterogeneous programming

#### Community Project Drives Language Enhancements

- Provides extensions to simplify data parallel programming
- Continues evolution through open and cooperative development



Direct Programming: SYCL/Data Parallel C++

Community Extensions

Khronos SYCL

ISO C++

#### SYCL ecosystem is growing



https://www.khronos.org/blog/sycl-2020-what-do-you-need-to-know

+ Celerity: SYCL on MPI+SYCL



#### ONEAP Industry Specification

#### spec.oneapi.com/oneAPI/

- Notices and Disclaimers
- <u>Contribution Guidelines</u>
- Introduction
- <u>Software Architecture</u>
- Library Interoperability
- oneAPI Elements
- Data Parallel C++ (DPC++)
- oneAPI Data Parallel C++ Library (oneDPL)
- oneAPI Deep Neural Network Library (oneDNN)
- oneAPI Collective Communications Library (oneCCL)
- oneAPI Level Zero (Level Zero)
- oneAPI Data Analytics Library (oneDAL)
- oneAPI Threading Building Blocks (oneTBB)
- oneAPI Video Processing Library (oneVPL)
- oneAPI Math Kernel Library (oneMKL)
- <u>Contributors</u>

## oneAPI Ecosystem Support



These organizations support the oneAPI initiative 'concept' for a single, unified programming model for cross-architecture development. It does not indicate any agreement to purchase or use of Intel's products. \*Other names and brands may be claimed as the property of others.

intel

## oneAPI: Open Accelerator Ecosystem

Freedom of Choice in Hardware Drives Productivity



"DPC++ and oneAPI helped us to develop much faster the accelerators for machine learning algorithms." – Chris Kachris, co-founder, InAccel

"If you like modern, standard C++ and you want to target GPUs or other accelerators, you will love SYCL!" – Marcel Breyer





Visualization of *easyWave* tsunami simulation application - Courtesy Zuse Institute Berlin (ZIB)

## Intel® oneAPI Toolkits and Components





#### Intel<sup>®</sup> oneAPI Tools



#### Built on Intel's Rich Heritage of CPU Tools Expanded to XPUs

A complete set of advanced compilers, libraries, and porting, analysis and debugger tools

- Accelerates compute by exploiting cutting-edge hardware features
- Interoperable with existing programming models and code bases (C++, SYCL, Fortran, Python, OpenMP, etc.), developers can be confident that existing applications work seamlessly with oneAPI
- Eases transitions to new systems and accelerators
- Using a single code base frees developers to invest more time on innovation

#### Available with paid Commercial Support

Latest version is 2023.2



#### Available Now

Visit <u>software.intel.com/oneapi</u> for more details Some capabilities may differ per architecture and custom-tuning will still be required. Other accelerators to be supported in the future.

## Analysis & Debug Tools

Get More from Diverse Hardware



	کی کی <b>Debug</b>	E Tune						
Intel <sup>®</sup> Advisor	Intel <sup>®</sup> Distribution for GDB	Intel® VTune™ Profiler						
<ul> <li>Efficiently offload code to GPUs</li> <li>Optimize your CPU/GPU code for memory and compute</li> <li>Enable more vector parallelism and improve efficiency</li> <li>Add effective threading to unthreaded applications</li> </ul>	<ul> <li>Multiple accelerator support with CPU, GPU and FPGA</li> <li>Enables deep, system-wide debug of Data Parallel C++ (DPC++), C, C++, and Fortran code</li> </ul>	<ul> <li>Tune for GPU, CPU, and FPGA</li> <li>Optimize offload performance</li> <li>Supports DPC++, C, C++, Fortran, Python, Go, Java or a mix of languages</li> </ul>						

#### Latest version available 2022.1



# A core set of high-performance libraries and tools for HPC

#### A complete set of proven developer tools expanded from CPU to XPU (accelerators)

TOOLKIT A core set of high-performance libraries and tools for building C++, SYCL and Python applications Intel<sup>®</sup> oneAPI Tools for IoT oneAPI HPC TOOLKIT IOT TOOLKIT Add-on DomainoneAPI Deliver fast Fortran, OpenMP & MPI Build efficient, reliable solutions that applications that scale run at network's edge **specific** Toolkits Intel<sup>®</sup> oneAPI AI Analytics Toolkit Intel<sup>®</sup> oneAPI Rendering intel intel oneAPI Toolkit RENDERING ANALYTICS Accelerate machine learning & data science pipelines with optimized DL frameworks & Create performant, high-fidelity high-performing Python libraries visualization applications Toolkit Intel<sup>®</sup> Distribution of OpenVINO<sup>™</sup> Toolkit **OpenVINO**<sup>®</sup> powered by oneAPI Deploy high performance inference & applications from edge to cloud

## Intel<sup>®</sup> oneAPI Toolkits

(accelerators) oneA

BASE

intel.

## Commercial Toolkits Deliver Priority Support (Paid Support Licenses)

#### Next Generation of Commercial Intel® Software Development Products

- Worldwide support from Intel technical consulting engineers
- Prior commercial tool suites, Intel<sup>®</sup> Parallel Studio XE and Intel<sup>®</sup> System Studio, transition to oneAPI products



27



## Intel<sup>®</sup> oneAPI Toolkits Availability

#### Get Started Quickly

Code Samples, Quick-start Guides, Webinars, Training

software.intel.com/oneapi





## Intel<sup>®</sup> oneAPI Toolkits – Proven Performance

#### **Top Takeaways & Proof Points**

- HPC Cross-architecture <u>Argonne National Labs</u> is running Exascale-class applications efficiently on current and future generations of Intel CPUs and GPUs
- HPC Cross-architecture <u>Zuse Institute Berlin (ZIB)</u> ported the tsunami simulation easyWave application from CUDA to Data Parallel C++ delivering performance across multiple architectures from multiple vendors
- HPC & AI <u>CERN uses Intel<sup>®</sup> DL Boost and oneAPI</u> to speed simulations with inference acceleration by nearly 2x without accuracy loss\*
- Hyper-real Visualization & AI Using Advanced Ray Tracing <u>Bentley Motors</u> <u>Limited's AI-based car configurator</u> processes 1.7M+ images with up to 10B possible configurations per model\*
- IoT <u>Samsung Medison accelerates ultrasound image processing</u> at the edge on multiple Intel<sup>®</sup> architectures for improved accuracy and fast diagnosis
- Major CSPs & Framework <u>endorse oneAPI</u> Microsoft Azure, Google Cloud, TensorFlow
- FPGA Using oneAPI, <u>Bittware</u> had its application running in days vs. what typically would take several weeks using Verilog or VHDL\*
- And more... 250+ applications developed with oneAPI tools > view <u>catalog</u>



Driving a New Era of Accelerated Computing

Innovation Leaders using Intel<sup>®</sup> oneAPI Cross-architecture Tools





Video [3:45]

<sup>\*</sup>Detailed slides per customer are noted in the oneAPI Customer Use Cases deck. Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy. See <u>Notices & Disclaimers</u> for more details.

## SYCLomatic: CUDA<sup>\*</sup> to SYCL<sup>\*</sup> Migration Made Easy

Choose where to run your software, don't let the software choose for you.



Open source SYCLomatic tool assists developers migrating code written in CUDA to C++ with SYCL, generating **human readable** code wherever possible

~90-95% of code typically migrates automatically ^  $^{1}$ 

Inline comments are provided to help developers finish porting the application

Intel<sup>®</sup> DPC++ Compatibility Tool is Intel's implementation, available in the Intel<sup>®</sup> oneAPI Base Toolkit



github.com/oneapisrc/SYCLomatic

## Codeplay oneAPI Plug-ins for Nvidia\* & AMD\*

Support for Nvidia & AMD GPUs to Intel® oneAPI Base Toolkit

#### oneAPI for NVIDIA & AMD GPUs

- Free download of binary plugins to Intel<sup>®</sup> oneAPI DPC++/C++ Compiler:
- Nvidia GPU
- AMD beta GPU
- No need to build from source!
- Plug-ins updated quarterly in-sync with SYCL 2020 conformance & performance

#### **Priority Support**

- Available through Intel, Codeplay & our channel
- Requires Intel Priority Support for Intel<sup>®</sup> oneAPI DPC++/C++ Compiler
- Intel takes first call, Codeplay delivers backend support
- Codeplay provides access to older plug-in versions



## GROMACS – Using oneAPI





Intel oneAPI Tools: Empowering GROMACS Cross-Architecture Development @IntelDevTools

,... "The part of oneAPI that is most important to me and my team is that, of course, it's an open standard. We are firm believers in open standards, particularly in the long run, because that means we can rely on it no matter what the vendors do. ...", Erik Lindahl; **Video 2** @sycl.tech

#### Click on the image to run the first video

## oneAPI Resources

#### software.intel.com/oneapi

Get Started

- software.intel.com/oneapi
- Documentation + dev guides
- Code Samples
- Intel<sup>®</sup> DevCloud



oneAPI

Developer Summit 2020

Register Now

#### Learn

- Training: Webinars & courses
- Intel<sup>®</sup> DevMesh Innovator Projects
- Summits & Workshops: Live & on-demand virtual workshops, community-led sessions
- Training by certified oneAPI experts worldwide for HPC & AI

#### Ecosystem

- Community Forums
- Intel<sup>®</sup> DevMesh Innovator Projects



 <u>Academic Programs</u>: oneAPI Centers of Excellence: research, enabling code, curriculum, teaching

#### Industry Initiative

- oneAPI.io
- oneAPI open Industry Specification
- Open-source Implementations



## Other useful Content Resources



Vectorization in LLVM and GCC for Intel CPUs and GPUs

Efficient Heterogeneous Parallel Programming Using OpenMP

ArrayFire Interoperability with oneAPI, Libraries, and OpenCL



#### Click on images to activate links & to subscribe

The plact your interact Office prev automated where prove the show the prove the show the Developer March 2022	Privery State Products In	nsights			**********				
PRODUCTS	DEVCLOUD	<u>TRAINING</u>	WEBINARS			Y	<u>'Ol</u>	JTI	JBI

Forwarded from a friend? Subscribe now  $\rightarrow$ 

#### **Featured Content**



#### **5 Outstanding Additions in SYCL**

SYCL 2020 offers C++ programmers 5 new features to take advantage of accelerators and the potential of open, cross-platform development. Find out what they are and how you benefit.

Read it →

intel. <sup>34</sup>

## Summary



- oneAPI cross-architecture, one source programming model provides freedom of XPU choice.
   Apply your skills to the next innovation, not to rewriting software for the next hardware platform.
- Intel<sup>®</sup> oneAPI Toolkit products take full advantage of accelerated compute by maximizing performance across Intel CPUs, GPUs, and FPGAs.
- Develop confidently with a proven set of crossarchitecture libraries and advanced tools that interoperate with existing performance programming models.

## Back Up Details about Intel<sup>®</sup> oneAPI Toolkits

#### Intel<sup>®</sup> oneAPI Base Toolkit Accelerate Data-centric Workloads

A core set of core tools and libraries for developing high-performance applications on Intel® CPUs, GPUs, and FPGAs.

#### Who Uses It?

- A broad range of developers across industries
- Add-on toolkit users since this is the base for all toolkits

#### Top Features/Benefits

- Data Parallel C++ compiler, library and analysis tools
- SYCLomatic / DPC++ Compatibility tool helps migrate CUDA code to C++ with SYCL
- Python distribution includes accelerated scikit-learn, NumPy, SciPy libraries
- Optimized performance libraries for threading, math, data analytics, deep learning, and video/image/signal processing

#### Intel<sup>®</sup> oneAPI Base Toolkit

Direct Programming	API-Based Programming	Analysis & debug Tools
Intel® oneAPI DPC++/C++ Compiler	Intel® oneAPI DPC++ Library oneDPL	Intel® VTune <sup>™</sup> Profiler
Intel® DPC++ Compatibility Tool	Intel® oneAPI Math Kernel Library - oneMKL	Intel <sup>®</sup> Advisor
Intel® Distribution for Python	Intel® oneAPI Data Analytics Library - oneDAL	Intel <sup>®</sup> Distribution for GDB
Intel® FPGA Add-on for oneAPI Base Toolkit	Intel® oneAPI Threading Building Blocks - oneTBB	
	Intel® oneAPI Video Processing Library - oneVPL	
	Intel® oneAPI Collective Communications Library oneCCL	
	Intel® oneAPI Deep Neural Network Library - oneDNN	intel
	Intel® Integrated Performance Primitives - Intel® IPP	ONEAPI BASE

#### Intel<sup>®</sup> one API Tools for HPC Intel<sup>®</sup> One API HPC Toolkit Deliver Fast Applications that Scale

#### What is it?

A toolkit that adds to the Intel<sup>®</sup> oneAPI Base Toolkit for building high-performance, scalable parallel code on C++, Fortran, SYCL, OpenMP & MPI from enterprise to cloud, and HPC to AI applications.

#### Who needs this product?

- OEMs/ISVs
- C++, Fortran, OpenMP, MPI Developers

#### Why is this important?

- Accelerate performance on Intel<sup>®</sup> Xeon<sup>®</sup> & Core<sup>™</sup> processors & Intel accelerators
- Deliver fast, scalable, reliable parallel code with less effort built on industry standards

#### Intel® oneAPI Base & HPC Toolkits

Direct Programming	API-Based Programming	Analysis & debug Tools
Intel <sup>®</sup> C++ Compiler Classic	Intel <sup>®</sup> MPI Library	Intel <sup>®</sup> Inspector
Intel® Fortran Compiler Classic	Intel® oneAPI DPC++ Library oneDPL	Intel® Trace Analyzer & Collector
Intel <sup>®</sup> Fortran Compiler	Intel® oneAPI Math Kernel Library - oneMKL	Intel <sup>®</sup> Cluster Checker
Intel® oneAPI DPC++/C++ Compiler	Intel® oneAPI Data Analytics Library - oneDAL	Intel® VTune™ Profiler
Intel® DPC++ Compatibility Tool	Intel® oneAPI Threading Building Blocks - oneTBB	Intel <sup>®</sup> Advisor
Intel® Distribution for Python	Intel® oneAPI Video Processing Library - oneVPL	Intel <sup>®</sup> Distribution for GDB
Intel® FPGA Add-on for oneAPI Base Toolkit	Intel® oneAPI Collective Communications Library oneCCL	
	Intel® oneAPI Deep Neural Network Library - oneDNN	intel
Intel® oneAPI <b>HPC</b> Toolkit + Intel® oneAPI <b>Base</b> Toolkit	Intel® Integrated Performance Primitives – Intel® IPP	ONEAPI HPC

Learn More

##